PTO/SB/44 (09-07)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,363,472

APPLICATION NO.: 09/972,797

ISSUE DATE : April 22, 2008

INVENTOR(S) : Dave Stuttard; Dave Williams; Eamon O'Dea; Gordon Faulds; John Rhoades; Ken Cameron; Phil Atkin; Paul Winser; Russell David; Ray McConnell; Tim Day and Trey Greer

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Related Foreign Data:

United Kingdom 9908199.4, filed on April 9, 1999.
United Kingdom 9908201.8, filed on April 9, 1999.
United Kingdom 9908203.4, filed on April 9, 1999.
United Kingdom 9908204.2, filed on April 9, 1999.
United Kingdom 9908205.9, filed on April 9, 1999.
United Kingdom 9908209.1, filed on April 9, 1999.
United Kingdom 9908211.7, filed on April 9, 1999.
United Kingdom 9908214.1, filed on April 9, 1999.
United Kingdom 9908219.0, filed on April 9, 1999.
United Kingdom 9908222.4, filed on April 9, 1999.
United Kingdom 9908225.7, filed on April 9, 1999.
United Kingdom 9908226.5, filed on April 9, 1999.
United Kingdom 9908227.3, filed on April 9, 1999.
United Kingdom 9908228.1, filed on April 9, 1999.
United Kingdom 9908229.9, filed on April 9, 1999.
United Kingdom 9908230.7, filed on April 9, 1999.

See Pages 2 and 3: Claims 2, 4 and 7 (corrections attached hereto).

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Claims 1, 2, 4 and 7 should read as follows:

Claim 1: A method of retrieving a data item from a memory unit in a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items and wherein the data processing apparatus includes a said memory unit in which data items are stored at addresses therein, and to which the plurality of processing elements have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

retrieving at least one data item stored at the transmitted target address in the memory unit;

transmitting the retrieved data item and associated transaction identification information to the processing elements in the array; and

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the retrieved data item.

Claim 2: A method of writing data items to a memory unit in a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items, and wherein the data processing apparatus includes the memory unit in which data items are stored at addresses therein, and to which the plurality of processing elements have access the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to all the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

transmitting transaction identification information to the processing elements in the array;

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, transmitting at least one data item to be stored in the memory unit at the target address; and

storing the transmitted data item at the target address in the memory unit.

Claim 4: In a data processing apparatus, a method of retrieving a data item from a memory unit in which data items are stored at addresses therein, said data processing apparatus further comprising an array of a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

retrieving at least one data item stored at the transmitted target address in the memory unit;

transmitting the retrieved data item and associated transaction identification information to the processing elements in the array; and

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the retrieved data item.

Claim 7: A method of writing data items to a memory unit in a data processing apparatus including the memory unit in which data items are stored at addresses therein, and an array of a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to all the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

transmitting transaction identification information to the processing elements in the array;

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, transmitting at least one data item to be stored in the memory unit at the target address; and

storing the transmitted data item at the target address in the memory unit.

UNITED STATES PATENT AND TRADEMARK OFFICE

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WASHINGTON, D.C. 20231
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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/972,797	10/09/2001	2183	5483	032658-018	17	204	38

CONFIRMATION NO. 3642

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UPDATED FILING RECEIPT

OC000000008382293

Date Mailed: 07/02/2002

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

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Domestic Priority data as claimed by applicant

THIS APPLICATION IS A CON OF PCT/GB00/01332 04/07/2000

Foreign Applications

UNITED KINGDOM 9908199.4 04/09/1999
UNITED KINGDOM 9908201.8 04/09/1999
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UNITED KINGDOM 9908219.0 04/09/1999

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UNITED KINGDOM 9908222.4 04/09/1999
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UNITED KINGDOM 9908229.9 04/09/1999
UNITED KINGDOM 9908230.7 04/09/1999

If Required, Foreign Filing License Granted 11/13/2001

Projected Publication Date: 10/10/2002

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Parallel data processing apparatus

Preliminary Class

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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is input into the PE register file **1061***b*. When the transaction ID is returned to the processing block, the processing elements compare the stored transaction ID with the incoming transaction ID, in order to recover the data.

Using transaction IDs in place of simply storing the accessed address information enables multiple memory accesses to be carried, and then returned in any order.

Booth multiplication is achieved using the B multiplexer **212**, which is shown in more detail in FIG. **14**. The B multiplexer **212** receives inputs **230** from the V and P registers and from the MEE **1602**. The B multiplexer **212** includes a Booth recode table **218** and a shift and complement unit **220**. The Booth recode table **218** receives inputs **224**, **226** from the two least significant bits of the S register and from a Booth register (S reg and Boothreg). Booth recoding is based on these inputs and the Booth recode table transforms these bits into shift, transport and invert control bits which are fed to the shift and complement unit **220**. The shift and complement unit **220** applies shift, transport and invert operations to the contents of the V register. The shift operation shifts the V register one bit to the left, shifting in a 0, and the transport and invert bits cause the possibly shifted result to be transported, inverted or zeroed or a combination of these.

FIG. **15** shows a block diagram of the alu **214** of the processor element shown in FIG. **13**. The alu **214** receives 10 bit inputs **234** from the A and B multiplexers **210** and **212**, and also receives inputs **244** and **246** from the BoothCarryIn and CarryReg registers. The alu **214** also receives instructions from the controller. The alu **214** includes a carry propagate unit **236**, a carry generate unit **238** and a carry select unit **242**. The alu also includes an exclusive OR (XOR) gate **250** for determining the alu result output. A CarryChain unit **240** receives inputs from Carry propagate unit **236** and the carry generate unit **238**, and outputs a result to the XOR gate **250**.

The various units in the alu **214** operate to carry out instructions issued by the controller.

The invention claimed is:

1. A method of retrieving a data item from a memory unit in a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items and wherein the data processing apparatus includes said memory unit in which data items are stored at addresses therein, and to which the plurality of processing elements have access, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing elenent concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and it the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

retrieving at least one data item stored at the transmitted target address in the memory unit;

transmitting the ~~at least one~~ retrieved data item and associated transaction identification information to the processing elements in the array; and

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the ~~or each~~ retrieved data item.

2. A method of writing data items to a memory unit in a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items, and wherein the data processing apparatus includes the memory unit in which data items are stored at addresses therein, and to which the plurality of processing elements have access the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to all the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

transmitting transaction identification information to the processing elements in the array;

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, transmitting at least one data item to be stored in the memory unit at the target address; and

storing the ~~at least one~~ transmitted data item at the target address in the memory unit.

3. A method as claimed in claim **2**, wherein processing elements store data items at respective regions of the target memory address.

4. In a data processing apparatus, a method of retrieving a data item from a memory unit in which data items are stored at addresses therein, said data processing apparatus further comprising an array of a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

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selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction, identification information;

retrieving at least one data item stored at the transmitted target address in the memory unit;

transmitting the ~~at least one~~ retrieved data item and associated transaction identification information to the processing elements in the array; and

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the ~~at least one~~ retrieved data item.

5. A method as claimed in claim **4**, wherein retrieved data is returned in the order in which the transaction identification information is produced.

6. A method as claimed in claim **4**, wherein the retrieved data is returned in the order in which it is retrieved from the memory.

7. A method of writing data items to a memory unit in a data processing apparatus including the memory unit in which data items are stored at addresses therein, and an array of a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned reqnires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to all the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

transmitting transaction identification information to the processing elements in the array;

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, transmitting at least one data item to be stored in the memory unit at the target address; and

storing the ~~at least one~~ transmitted data item at the, target address in the memory unit.

8. A method as claimed in claim **7**, wherein processing elements store data items at respective regions of the target memory address.

9. A data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, data storage means for storing data items for access by the processing elements, and control means for controlling access to the storage means in accordance with a method as claimed in claim **8**.

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